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Amorphous SiO_x nanowires catalyzed by metallic Ge for optoelectronic applications

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ABSTRACT

Amorphous SiO_x nanowires, with diameters of ∼20 nm and lengths of tens of μm, were grown from self-organized GeSi quantum dots or GeSi alloy epilayers on Si substrates. The morphologies and yield of these amorphous nanowires depend strongly upon the synthesis temperature. Comparative experiments indicate that the present SiO_x nanowires are induced by metallic Ge as catalysts via the solid liquid solid growth mechanism. Two broad peaks centered at 410 nm and 570 nm were observed in photoluminescence spectrum, indicating that such SiO_x nanowires have the potential applications in white light-emitting diodes, full-colour display, full-colour indicator and light sources.

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1. Introduction

Nanowires have shown great potential as building blocks for future nanoscaled-devices in nanoelectronics and optoelectronics due to their higher integration density than other conventional materials [1–3]. Various nanowires, such as Si [4], ZnO [5], ZnS [6,7], GaN [8], GaP [9] and SiO_x [10] nanowires, have been synthesized by different methods. Among them, SiO_x nanowires attract special attention in optoelectronic applications because of their high intense and stable blue light emission at the room temperature [11,12] and their potential applications in the field of light localizations [11,13], low dimensional waveguides [11,13,14], and scanning near-field optical microscopy [11,14,15]. Until now, various methods, such as laser ablation [11], chemical vapor deposition [16] or thermal evaporation [17,18], have been developed to controllably synthesize high-purity SiO_x nanowires. All these growth methods can be classified to two growth mechanisms: catalytic growth and non-catalytic growth. To satisfy the requirement for device application, one important issue is to precisely control the location and the size of the nanowires [19]. Compared to the non-catalytic growth, one distinct feature is that the catalytic growth has the potential to control the position and size of the nanowires, because the diameter and location of the nanowires are controlled by the diameter and location of the catalysts. The catalytic growth method can fall into two main growth mechanisms: vapor liquid solid (VLS) [20] and solid liquid solid (SLS) [21] growth mechanisms. In the SLS mechanism, the liquid metallic catalysts remain on the surface of the Si substrates during the entire growth process and the substrate itself serves as the Si source [22]. Generally, the SLS growth mechanism is an attractive and high-quantity method for producing SiO_x nanowires as it is a simple and effective process.

Metallic catalysts, such as Pt [23], Au [24], Fe [11], Cu [25], Co [26] and Ni [21], have been used for growing SiO_x nanowires. Generally, such metallic catalysts may incorporate into the nanowires during the nanowire growth [27]. Especially, such metallic catalysts may left in nanowires and trap electrons and holes and in turn result in serious contamination in the practical application for electronic and optical processing [28]. Therefore, searching for new catalysts is still a great challenge to obtain highly efficient and uncontaminated catalysts. In this regard, Ge, as an attractive candidate, could offer good material compatibility and facile integration with conventional Si-based nanostructured circuits. The Si/Ge system has been a globally focused topic for years because their well-controlled fabrication process for integrated Si-based circuits makes the realization of spintronics and quantum computation possible [29]. For instance, GeSi quantum dots (QDs), as its typical nanostructures, have received great attention because of their distinguished electric and optic performances which can be used for high-performance field-effect transistors [30] and infrared detectors [31].

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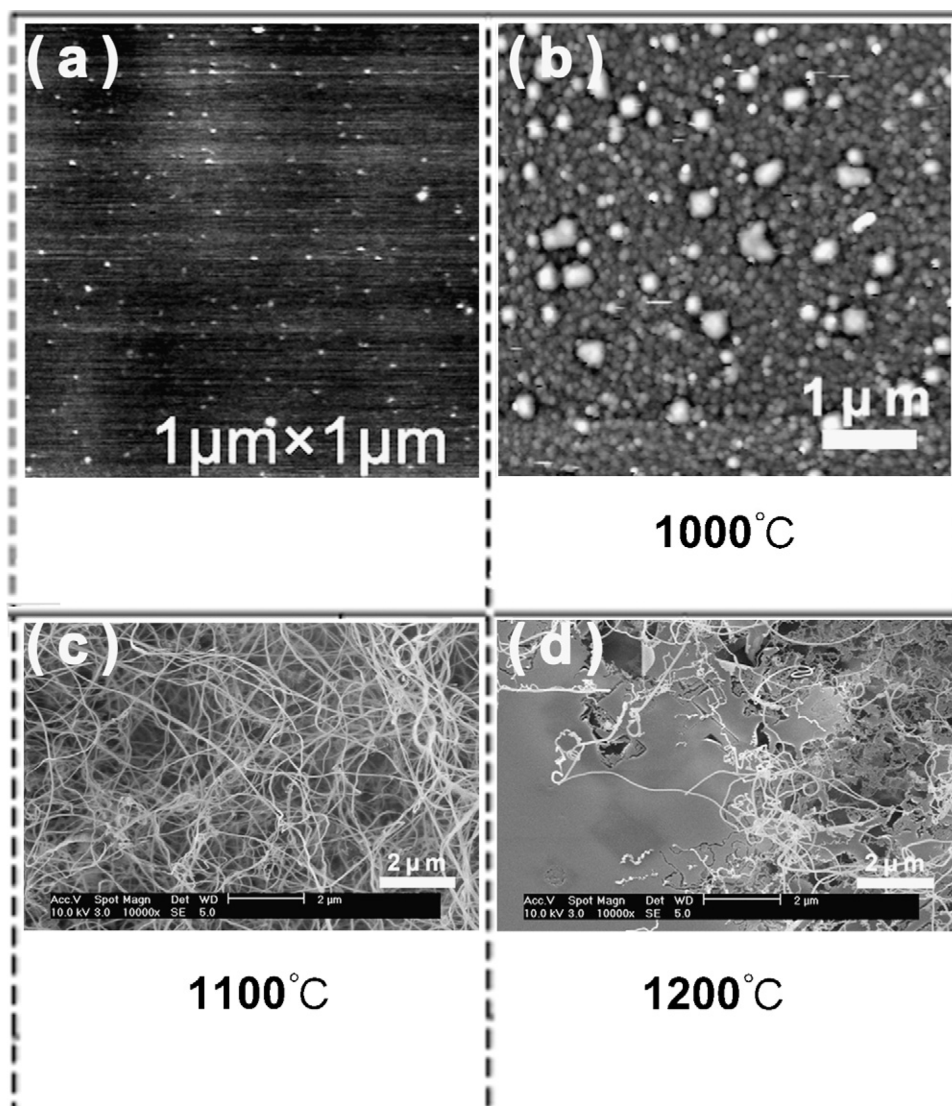

Fig. 1. (a) AFM image of a GeSi QD sample grown by MBE. (b) Large islands formed on the GeSi QD sample after annealing at 1000 °C. (c) and (d) SEM images of the SiO_x nanowires grown on the GeSi QD sample after annealing at 1100 °C and 1200 °C, respectively.

In this study, the SiO_x nanowires with diameters of ~20 nm and length of tens of μm were produced by directly annealing Ge(Si) QDs on Si substrates surrounded by a forming gas (95% N_2 and 5% H_2) at the atmospheric pressure. Based on carefully designed comparative experiments, we demonstrate that Ge is an excellent catalytic candidate for inducing SiO_x nanowires via the SLS growth mechanism. The photoluminescence measurement of the obtained SiO_x nanowires shows two emissions, centered respectively at 410 nm (blue light emission) and 570 nm (yellow light emission), suggesting that our SiO_x nanowires have potential applications in full-colour displays, full-colour indicators and lighting sources.

2. Experimental procedures

The growth of GeSi QDs on the Si (1 0 0) substrates was carried out in a solid source molecular beam epitaxy (MBE) system (Riber Eva-32) with two electron beam evaporators for Ge and Si sources, respectively. The base pressure of the system is better than 5×10^{-10} Torr. The substrates were chemically cleaned by the *Shiraki* method [32]. The native oxide on the substrate was desorbed at 1000 °C for 10 min in the growth chamber. The substrate temperature was then lowered to 460 °C, and an 80 nm thick Si buffer layer was grown at a growth rate of 0.05 nm s^{-1}. The substrate temperature was then raised to 650 °C for the GeSi QD growth in which a Ge layer with a nominal thickness of 0.4 nm was deposited onto the buffer layer at a grow rate of 0.01 nm s^{-1} (Noted that, although Ge is deposited on the Si substrates, GeSi quantum dots are expected to be formed due to the diffusion of Si into the dots [33]).

The synthesis of SiO_x nanowires was carried out in an annealing furnace system equipped with a temperature controller and quartz tube. Three temperatures (namely 1000 °C, 1100 °C and 1200 °C) were chosen to synthesize SiO_x nanowires. The annealing furnace was heated to the set temperature in the presence of the forming gas (95% N_2 and 5% H_2) for eliminating the unwanted impure gas out of the quartz tube. The quartz boat containing GeSi QD samples was then put into the middle of the furnace tube and annealed for 30 min under the forming gas with a flow rate of 100 L h^{-1}, followed by naturally cooled to the room temperature.

The morphologies of the as-grown GeSi QD samples were characterized by atomic force microscopy (AFM, Solver P47-SPM-MDT) with the contact mode in air. The morphological and structural characteristics of synthesized products were comprehensively characterized by scanning electron microscopy (SEM, JEOL JSM-6701F), transmission electron microscopy (TEM, Philips F20 and FEI Tecnai F30, equipped respectively with energy dispersive spectroscopy (EDS) and electron energy loss spectroscopy (EELS)). Photoluminescence measurement (PL, Jobin Yvon 1000) was carried out using a 325 nm laser as the excitation source at the room temperature.

3. Results and discussion

Fig. 1(a) is a typical AFM image of an as-grown GeSi QD sample with the nominal Ge layer of 0.4 nm and shows small dots with diameters of 30–40 nm and heights of 2–3 nm. After annealed at 1000 °C for 30 min under the forming gas, the size of dots increases

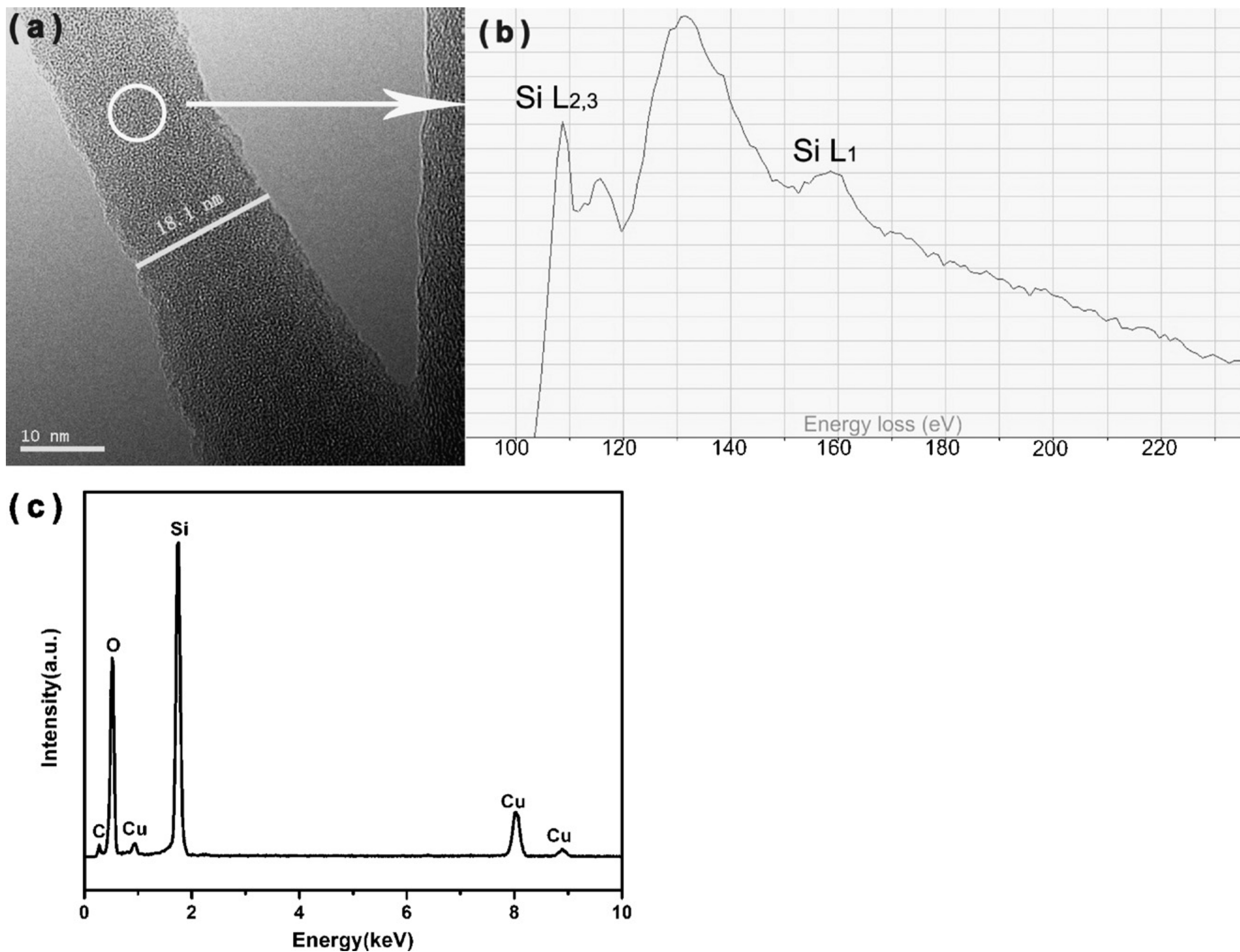

Fig. 2. (a) HRTEM image of a section of a typical SiO_x nanowire. The circle indicates the area where EELS is measured. (b) Si-$L_{2,3}$ ELNES of a single SiO_x nanowire. (c) EDS spectrum taken from a typical nanowire.

(with diameter of several hundred nm and height of dozens of nm) and no other features, such as nanowires, were observed, as evidenced by the AFM observation (refer to Fig. 1(b)). When the annealing temperature increases to 1100 °C, dense nanowires randomly formed on the substrate were observed, as shown in Fig. 1(c). Their length is in the order of tens of μm with a diameter of ~20 nm. With further increasing the annealing temperature to 1200 °C, the density of nanowires is decreased (refer to Fig. 1(d)) when compared with those nanowires formed by annealing at 1100 °C.

In order to understand the detailed structural and chemical characteristics of synthesized nanowires, high resolution TEM (HRTEM) investigations on individual nanowires were carried out. Fig. 2(a) is a HRTEM image taken from a section of a typical nanowire and shows the pure amorphous nature. To understand their electronic structure and oxidation state of such amorphous nanowires, EELS analysis is employed [34,35]. Fig. 2(b) is an EELS profile taken from a region shown in Fig. 2(a), in which the Si L_{23} peak with onset edge located at energy 108.4 eV is higher than that of the Si L_{23} peak of elemental Si at energy of 99.8 eV, further confirming the existence of Si in the nanowire and its oxide nature. The peak of 115 eV can be attributed to the excitation of 2p electrons into the $6a_1$ molecule orbits of the SiO_4 tetrahedron [36]. The broad peak at 132 eV originates from the inner-wall resonance. The Si L_1 edge is about 160 eV [36]. According to the reference EELS spectrum of SiO_x [37], the nanowire can be verified as amorphous SiO_x. To further determine the ratio of Si and O in SiO_x nanowires, EDS was employed and an example was shown in Fig. 2(c). The quantity analysis reveals that the atomic ratio of Si and O is approximately 1:1.8. The C and Cu signals shown in EDS come from the TEM grid.

To clarify the growth mechanism of our SiO_x nanowires, a QDs-free Si substrate and GeSi QD samples with thicker nominal deposited Ge (0.8 nm and 1.2 nm) were annealed in the identical synthesis condition as mentioned above. No nanowires were observed on bare Si substrate. This result indicates that the GeSi QDs are essential catalysts for growing our nanowires, which can be further confirmed by the formation of dense nanowires on the GeSi QD samples with thicker nominal deposited Ge, as shown in Fig. 3(a) and (b). It should be noted that the metal oxide may catalyze the growth of SiO_x nanowires [38]. Since the GeSi QDs was inevitably oxidized due to exposure in the air, the possibility of GeO_x being a catalyst should also be examined. To clarify this, we deposited GeO_x on the Si substrates in a magnetron sputtering system and the as-sputtered samples were annealed in the same manner as the GeSi QD samples. No nanowires were observed on the Si substrates that contain GeO_x. Based on this result, we believe that our SiO_x nanowires must be catalyzed by metallic Ge, rather than ionic Ge. To further verify this, GeSi alloyed epilayers with 30 nm thickness were grown by MBE and were also annealed to synthesize SiO_x nanowires. Fig. 3(c) is the AFM image of the surface of such a GeSi alloyed epilayer and shows a very smooth film surface with the root-mean-square (RMS) surface roughness of ~0.3 nm. After annealing, SiO_x nanowires were formed on the Si substrates, as shown in Fig. 3(d). To further verify the position of the Ge catalysts related to the nanowires, cross-section TEM specimens

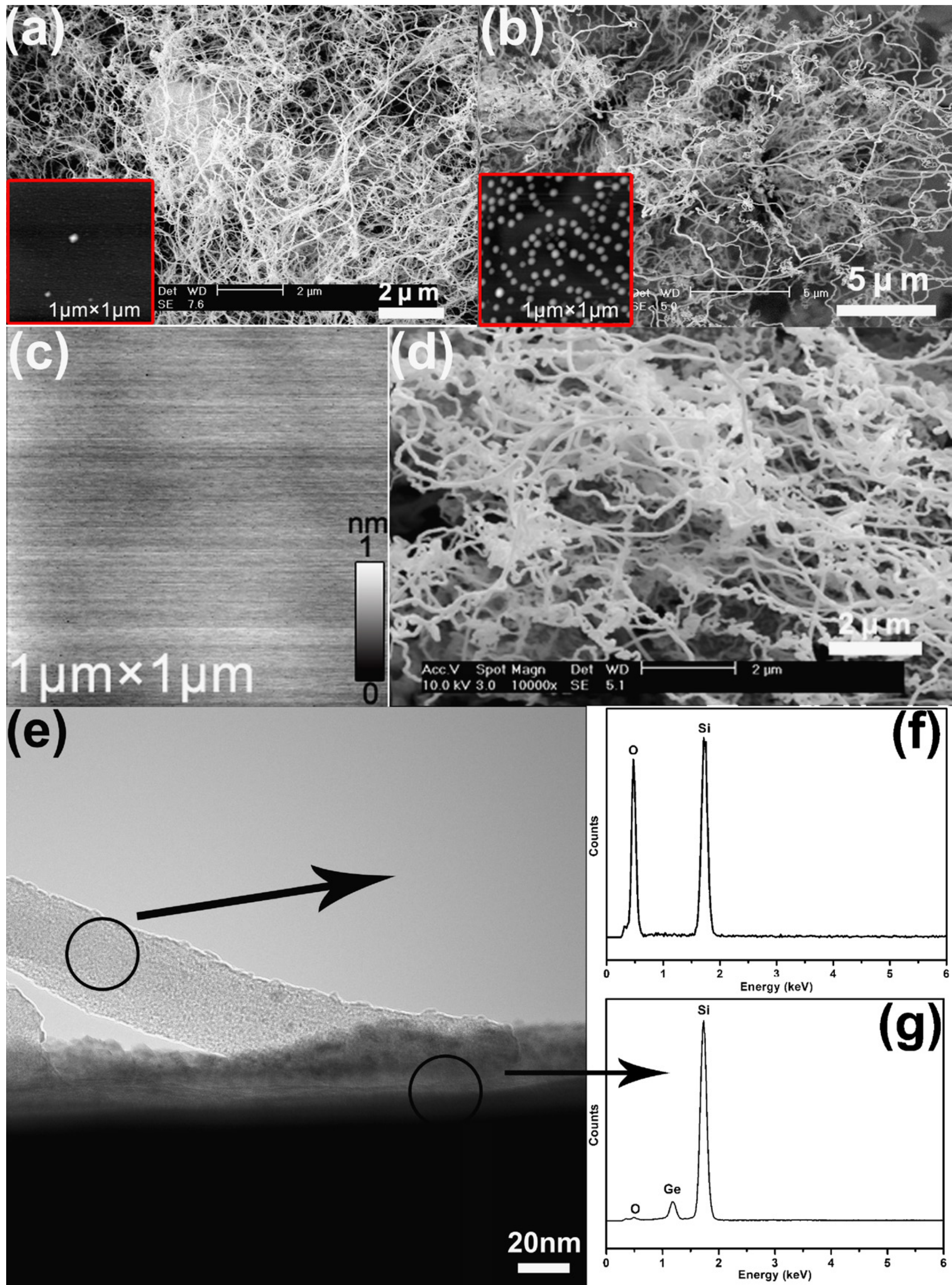

Fig. 3. (a) and (b) SEM images of SiO_x nanowires grown on GeSi QD sample with thicker nominal deposited Ge (0.8 nm and 1.2 nm), respectively. The insets are the AFM images of the as-grown GeSi QD samples. (c) AFM image of a GeSi epilayer sample grown by MBE. (d) SEM image of SiO_x nanowires grown on GeSi alloy epilayer sample. (e) Cross-section TEM image of annealed sample. (f) and (g) EDS plots corresponding to the nanowire and GeSi alloy regions, respectively.

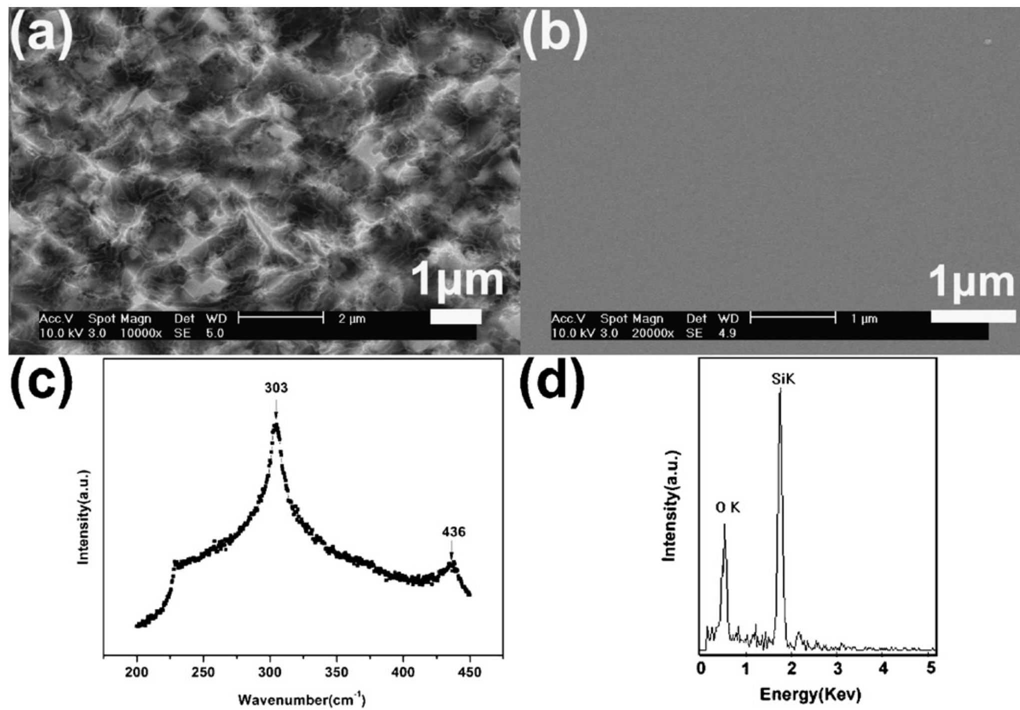

Fig. 4. (a) and (b) SEM images of bigger GeSi QD sample and bare Si substrate annealed at 1200 °C, respectively. (c) and (d) Raman and EDS spectrum of the pit from a GeSi QD sample annealed at 1200 °C.

of the annealed GeSi QD sample were prepared and investigated. An example is shown in Fig. 3(e), where a single SiO_x nanowire was initiated from a thin film attached with the substrate. Their corresponding EDS analyses confirmed that the nanowire has a composition of Si and O (refer to Fig. 3(f)) and the thin film contains mainly Si and Ge (refer to Fig. 3(g)). Based on these comparative analyses, it is anticipated that the GeSi alloy play a key factor for the nanowire growth. It is believed that the GeSi should be in the liquid state because the synthesized temperature is higher than the melting temperature of GeSi bulk alloys based on the GeSi phase diagram. Moreover, as mentioned earlier, for nanowires synthesized at 1200 °C, their density is lower than nanowires synthesized at 1100 °C. Also, a large quantity of pits was seen on the surface of the substrate annealed at 1200 °C (refer to Fig. 1(d)). Although we cannot see the pits on the substrate annealed at 1100 °C due to the high density of SiO_x nanowires, we can still reasonably predict the existence of pits in this case. We also note that Park et al. [22] reported that the higher temperature would induce higher density of SiO_x nanowires in the SLS growth mechanism because of stronger Si diffusion, although, in our case, an abnormal phenomenon was found, i.e. the higher temperature induced a lower density of SiO_x nanowires. We anticipated such a phenomenon should be related to the nature of Ge as the chosen catalysts. To determine whether the pit formation is related to the existence of GeSi QDs and their density, a comparative experiment was designed, in which a bare Si substrate and a Si substrate with larger GeSi QDs (with a nominal Ge layer of 1.2 nm) were annealed at 1200 °C under the identical condition (compared to that of GeSi QD sample with the nominal Ge layer of 0.4 nm), and their typical characteristics were shown in Fig. 4. As can be seen, a rough surface has been resulted by the Si substrate containing GeSi QDs [refer to Fig. 4(a)], mostly likely due to the generation of pits. In strong contrast, the surface of the bare Si substrate is remarkably flat [refer to Fig. 4(b)]. The comparison of Fig. 4(a) and (b) indicates that the existence of GeSi QDs is responsible for the pit formation, which may be critical for the growth of SiO_x nanowires. And the larger GeSi QDs induced more and larger area pits from our extensive low resolution SEM characterization. Both the micro-Raman spectrum and EDS were used to further characterize the nature of the pits. Raman spectrum (Fig. 4(c)) collected from the pit region shows that two peaks, centered at 303 cm^{-1} and 436 cm^{-1}, are respectively assigned to the second-order transverse acoustical phonon and first-order longitudinal optical phonon of Si without any feature peaks of Ge [30], indicating no Ge in the pit. This result was also confirmed by the EDS analysis (refer to Fig. 4(d)), in which only Si and O signals can be seen. Based on these experimental data, pits may be formed in two possible ways: (1) Ge, as a catalyst, promotes the depletion of Si [39]; or (2) Ge diffuse into Si substrate to form liquidized Ge–Si alloy which may evaporate because the synthesis temperature of 1200 °C is much higher that the melting temperature of Ge–Si alloy (938 °C). To understand which mechanism dominates in our case, we use the Clausius–Clapeyron equation, applicable to liquid/gas equilibrium curves, to determine the vapour pressure as a function of the annealing temperature [40]. The equation can be expressed as follows:

$$\ln \frac{p_2}{p_1} = \frac{-H_{vap}}{R} \left[\frac{1}{T_2} - \frac{1}{T_1} \right],$$

where H_{vap} is enthalpy of the vapour, R is the gas constant, T is the absolute temperature, and p is vapour pressure. As can be seen, the vapour pressure increases with increasing temperature. The higher temperature will induce severer evaporation, and finally the boiling phenomenon happens when the vapour pressure is equal to the ambient pressure [41]. As a consequence, it is anticipated that the absence of Ge in pit position is due to the evaporation of liquidized Ge–Si alloy. Since Ge can diffuse into the Si substrate, the Ge–Si alloy evaporates and consumes Si to form the coarse surface of the Si substrate, and finally results in the formation of pits. Since the SiO_x nanowires were induced by the Ge catalysts, we anticipate that the lower density of SiO_x nanowires at 1200 °C can be attributed to the decrease of catalysts, i.e. evaporation of liquidized GeSi alloy.

Although it is clear that our SiO_x nanowires were catalyzed by metallic Ge, the evolution of our SiO_x nanowires are still not clear as there are generally two possible mechanisms. (1) The Si

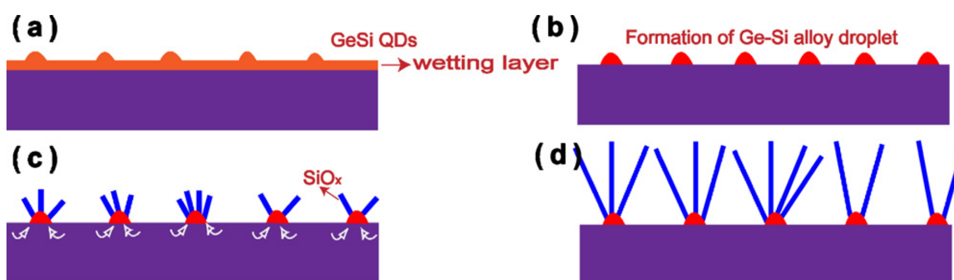

Fig. 5. Schematic description of proposed mechanism for nanowire growth: (a) GeSi QD samples grown by MBE. (b) Ge–Si alloy droplet formed at high temperature. (c) Si atoms diffusion to GeSi droplet, deposit to form Si nanowires and oxidation of Si nanowires. (d) Growth of SiO_x nanowires.

nanowires may be firstly nucleated on the catalysts after Si diffuses into the catalyst. And then the residual oxygen in the tube furnace reacts with the Si nanowire and oxides to create a SiO_x shell until Si nanowire's complete oxidation [42,43]. (2) The diffused Si atoms on the substrate react with the residual oxygen in the tube furnace to form SiO_x as the sources. The catalysts as preferential sites absorb the SiO_x source to reach supersaturation and then the SiO_x nanowires precipitate from the catalysts to form entire nanowire [44]. To determine the possible mechanism for our case, we note that if the oxidation occurs at the former scenario, the oxide nanowires should contain Ge, since GeSi intermixing is significant at high temperature [45,46]. The fact that no Ge can be detected from the synthesized nanowires (confirmed by both EELS and EDS) suggests that our SiO_x nanowires should be directly formed from the Ge–Si alloy droplets, that is, the SiO_x nanowire growth should be governed by the latter scenario. Based on the experimental results outlined above, our SiO_x nanowire growth should be catalyzed by metallic Ge through the SLS model and their evolution can be schematically illustrated in Fig. 5. At the high growth temperature, the GeSi QDs would be transformed to Ge–Si alloy droplets, as illustrated in Fig. 5(a) and (b). Since trace of oxygen was inevitable in our annealing tube furnace, the Si atoms on the substrate were oxidized to form SiO_x clusters, which would be absorbed to the Ge catalysts. The SiO_x would precipitate from the solution to form SiO_x nanoparticles on the catalyst, where the nanoparticles act as nucleation sites and initiate the growth of the SiO_x nanowire (refer to Fig. 5(c)). Consequently, nanowires could be grown from catalysts (Fig. 5(d)). Since the diameters of the nanowires are much thinner than the size of the catalysts, we anticipate that each catalyst (originated as a QD) may induce several nanowires.

Since SiO_x nanowires possess unique optoelectronic properties [11,12], PL measurements were carried out for our synthesized SiO_x nanowires. Fig. 6 shows a typical PL spectrum obtained from synthesized SiO_x nanowires. Two broad PL peaks, centered respectively at 412 nm (3.0 eV) and 570 nm (2.2 eV), were observed. Nishikawa et al. [47] observed several luminescence bands in various high purity silica glasses, with different peak energies ranging from 1.9 to 4.3 eV under a 157 nm excimer laser. It reveals that the 3.0 eV peak is ascribed to the two-fold coordinated Si lone pair centers (O–Si–O) and the weak O–O bonding as a preexisting oxygen defect [47]. This defect is due to high oxygen deficiency during the nanowire synthesis. The 3.0 eV PL peak was also observed in SiO_x nanowires [11], which was believed to be due to this type of oxygen defects. The 570 nm yellow emission peak was rarely observed in previous reported SiO_x nanowire PL spectra [11,15,48,49]. The 570 nm luminescence peak was found from Ge microcrystal embedded in SiO_2 glassy matrices [50], which was attributed to the quantum confinement of electrons and holes in Ge microcrystal. However, in our experiment, no Ge nanoparticles were found in the SiO_x nanowires through our extensive TEM observations. As a consequence, the 570 nm PL peak should be due to other mechanism. To understand this, we note that Chen et al. [51] reported a 570 nm peak in an electroluminescence spectrum of Ge-implanted Si-rich SiO_2, different from the Si-implantation, which probably originated from the E'_δ center [52], i.e. excess Si/O vacancy complex related defects. Based on this, we anticipate that the 570 nm PL peak found in our SiO_x nanowires should be attributed to the defects related E'_δ center. It is of interest to note that our SiO_x nanowires possess both blue and yellow emissions. Since the white light-emitting diodes (LEDs) may be achieved by the combination of a blue LED and a yellow phosphor [53], our SiO_x nanowires therefore may have potential applications in white LEDs.

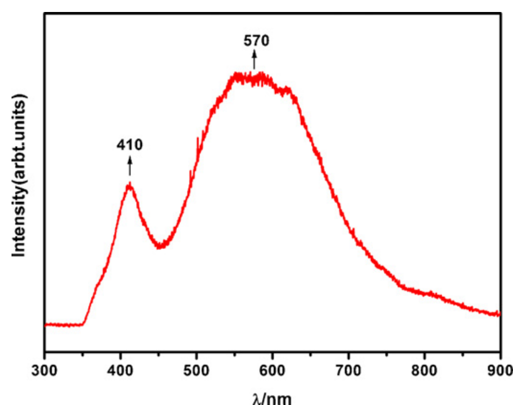

Fig. 6. PL spectrum of SiO_x nanowires showing two broad peaks centered at 410 nm and 570 nm.

4. Conclusions

Through comparative growth experiments and detailed structural characterizations, metallic Ge has been demonstrated as an effective catalyst for the growth of SiO_x nanowires on Si substrates. Such a catalyst may avoid catalyst contamination caused by their unconsciousness left in the nanowires. The blue and yellow light emissions were observed which could be attributed to the defect centers of the oxygen deficiency in the nanowires, which may be used in white light-emitting diodes, full-colour display, indicator and light sources.

Acknowledgements

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